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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,232	02/09/2004	Yoshiki Okumura	1614.1383	3164

21171 7590 05/02/2006

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EXAMINER	
ZAMAN, FAISAL M	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,232	OKUMURA, YOSHIKI	
	Examiner	Art Unit	
	Faisal Zaman	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5* is/are allowed.

6)☒ Claim(s) *6-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim 6 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 6-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nix (U.S. Patent No. 4,897,810) in view of Alwais (U.S. Patent No. 6,362,675).

Regarding Claim 6, Nix discloses a status bit setting circuit (Nix, title, abstract) comprising:

An inverting output part generating an output which is inverted each time that a predetermined status is detected (Nix, Figure 1, item 18, Column 2 lines 24-27, and Column 4 lines 9-52, the "IN" signal in Nix [see Column 3, lines 7-10] is considered equivalent to the predetermined status as stated in the current application);

State inversion transition parts having states inverted in sequence by the output of said inverting output part (Nix, Figure 1, items 66 and 68, Column 5, lines 37-45 and lines 58-66); and

A status bit setting part setting a predetermined status bit by detecting a process of propagation of the inversion transition in said state inversion transition parts (Nix, Figure 1, items 70, 72, 74, Column 4, lines 25-30, the signal sent to the microprocessor indicating an interrupt event in Nix [see Column 1, lines 29-36 and Column 2, lines 28-32] is considered equivalent to the status bit in the current application).

Nix does not expressly disclose wherein said state inversion transition parts comprise edge-triggering type devices.

In the same field of endeavor (e.g. detection of state changes in a data processing system), Alwais teaches state inversion transition parts, comprising edge-triggering type devices (Alwais, Figure 2, item 32, Column 4, lines 40-43), having states inverted in sequence by the output of an inverting output part (Alwais, Figure 2, item 54, Column 4 line 63 – Column 5 line 3).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Alwais' teachings of detection of state changes in a data processing system with the teachings of Nix, for the purpose of accurately detecting every state change in the input signal. Nix provides motivation to combine by stating it would be desirable to provide an asynchronous interrupt status bit circuit which guarantees that no interrupting conditions are missed and that no single interrupting condition is indicated twice (see Nix, Column 1, lines 46-50).

Regarding Claim 7, Nix discloses the status bit setting circuit further comprising a status detection canceling part (Nix, Figure 1, item 24, Column 4, lines 36-38)

detecting the process of the inversion transition in said state inversion transition parts, and generating a signal canceling a status detection state (Nix, Column 2, lines 32-39).

Regarding Claim 8, Nix discloses wherein said status bit setting part detects a completion of the propagation of the inversion transition and cancels the setting of the predetermined status bit (Nix, Figure 2, items (b) and (c), when the READ signal in Nix is set from the high to low level, the DBX signal also is set to the low level [ie. is cancelled], see Column 5 lines 50-57).

Regarding Claim 9, Alwais discloses wherein said state inversion transition parts have the states alternately inverted in sequence in response to a rising edge and a decaying edge of a predetermined read out signal (Alwais, Figure 2, item 32; ie. it is well known in the art that this is how a D flip flop operates since it is an edge-triggered flip flop, as evidenced by "Flip-flop (electronics)" by Wikipedia.org, cited below under Relevant Art).

The motivation utilized in the combination of Claim 6, super, applies equally as well to Claim 9.

Regarding Claim 10, Nix discloses the status bit setting circuit further comprising a bus driver (Nix, Figure 1, item 20, Column 4, lines 12-16) enabling reading out of the predetermined status bit externally only during an interval in which a predetermined read out signal is active (Nix, Figure 2, items (b) and (c), Column 5, lines

46-57, only when the READ signal is active [ie. at the high level], the DBX signal is sent to the microprocessor).

Allowable Subject Matter

1. **Claims 1-5** are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claims 1, 2, and 5, the prior art discloses apparatus for retaining signals in state holding parts (ie. flip-flop circuits). The prior art also discloses apparatus for comparing signals of two different states for the purpose of indicating the status of an incoming signal (ie. an exclusive-OR circuit). However, the organization of the different comparing parts in the claim are not disclosed in the prior art. The claims disclose the use of multiple comparing parts to compare the signals of the multiple state holding parts. The prior art, however, uses a single comparator (ie. a differential comparator) for this purpose.

Regarding Claims 3 and 4, the prior art does not disclose a state detection signal clearing part which compares the states of multiple input signal and outputs a state detection signal clearing signal when the states are different from one another.

Relevant Art/Prior Art of Record

2. "Flip-flop (electronics)", Wikipedia.org, <http://en.wikipedia.org/wiki/Flip-flop_(electronics)>, retrieved from the Internet on 4/27/2006 is cited as Relevant Art.

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Uede et al. (U.S. Patent No. 4,247,855) discloses a circuit that includes a state change detection circuit which is composed of two D-flip-flops and an exclusive-OR circuit. Takezoe et al. (U.S. Patent No. 4,500,953) discloses a data transfer abnormality processing system. Kitada (U.S. Patent No. 4,763,248) discloses a microcomputer with a detecting function of a memory access error. Ogata (U.S. Patent No. 4,829,467) discloses a memory controller including a priority order determination circuit. Tomioka et al. (U.S. Patent No. 4,870,345) discloses a semiconductor integrated circuit which includes cascaded asynchronous sequential logic circuits. Hillis et al. (U.S. Patent No. 5,118,975) discloses a circuit which includes multiple comparators and a state change detection circuit. Davis et al. (U.S. Patent No. 5,754,764) discloses a combination of input/output circuitry and local area network systems. Anderson et al. (U.S. Patent No. 5,815,733) discloses a system for handling interrupts in a computer system using an ASIC reset input line coupled to a set of status circuits for presetting values in the status circuits. Suetake et al. (U.S. Patent No. 5,822,557) discloses a pipelined data processing device having improved hardware control over an arithmetic operations unit. Haban (U.S. Patent No. 6,779,125) discloses a UART which can receive a clear to send (CTS) signal.

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

fmz

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
4/28/06